

d = 1 1 1

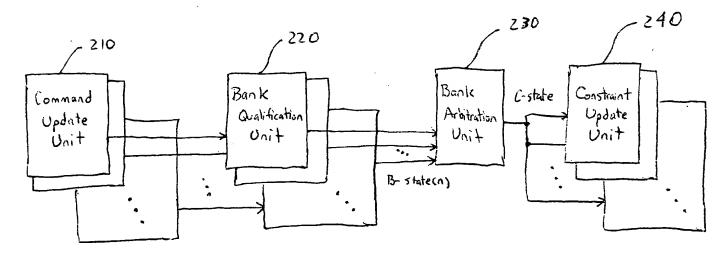
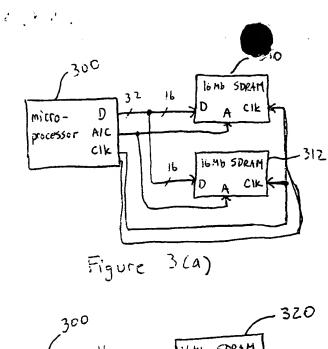
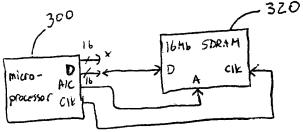
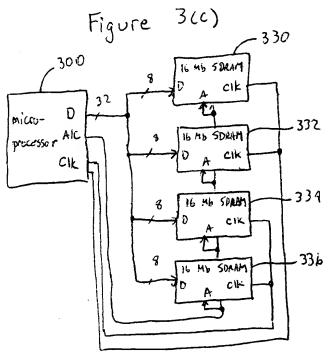


Figure Z

Sign 1







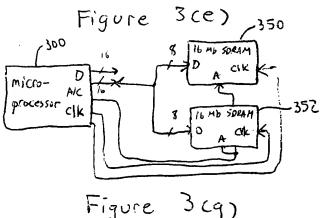


Figure 3 cg)

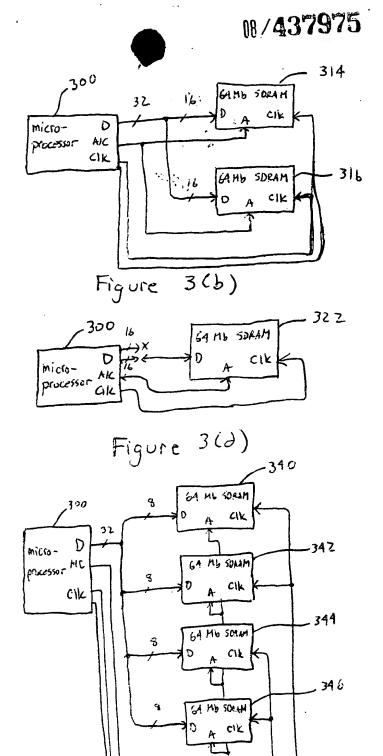
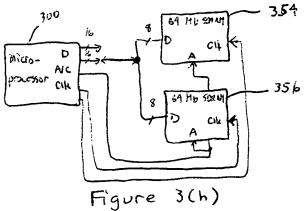


Figure 3 (f)



MOP XXXXXXX 00100 × stores loads 8 × 1500000 8 1FFF NOP NOP mode register set NOP MNOP MNOP <u>о</u> POWER · Precharge NOP NOP time -7777777 XXXXXXX XXXXXXX 00000000 XXXXX × Controller Return bus Request Controller Return bus Grant Controller Input bus SDRAM Clock Command Address Data Output to pad Controller Clack Controller Return bus Active Row O Word Address Active Row 1 Read Window Restart go Sample Reset Drive Ready

Figure 9(a)

00100

80000

00004

00000

time 1

XXXXX

Word Address

8

STORES

1500000	00000000    NOP   ACT   NO   IFF   NO   IFF	000 XXX
controller Clock	Restart go Restart go Ready Controller Input bus Controller Return bus Request Controller Return bus SORAM clock Command Address Data Outputo pad Drive Read Window	Sample Active Rowo Active Rowl

NOP 1FFF

8000

080

1FFF

, 8000

ACT 0800

0004

1FFF

0000

00000000

00000000

PRE

WRITE

WRITE NOP

WRITE

WRITE NOP

00000000

}€ }4

Figure 4(b)

LOADS

) )	1700000   1750000   1800000   1800000   1800000
entroller clock	
Reset	
Restart go	
Ready	
patroller Input bus	W XXXXXXXXX W XXXXXXXXX W XXXXXXXXXX
3	
cottoller Return bus Garact	
Controller return 605	00000000
SDRAM clock	
Command	NOP ACT NOP RO NOP RD ACT RO NOP RO PRE NOP PRE NOP NOP
Adres	1FFF (0000 (1FFF (0000 (1FFF (0004 (1FFF (0008 (0004 (1FFF (0800 (0004 (1FFF (0800 (1FFF (1FFF (0800 (1FFF (1FFF (0800 (1FFF (1FFF (0800 (1FFF (
	The second secon
Jara	3
output to pad	8 6 L. 9 xxxxxxxx 8
	0
Samle	
Active Rivin	xxx ooo xxx
ACHVP Raw )	xxx xxx
Word Address	00100 A0000 A00004 A00008 A00004 A00100

time +